Short Papers

Wide-Band GaInAs MISFET Amplifiers

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Abstract—**We present the first reported results on wide-band GaInAs MISFET amplifiers. Using 1-μm-gate-length, 0.56-mm-gate-width GaInAs MISFET's, we obtained (a) a power output of 230±30 mW (0.41 W/mm) with 33±3 percent power-added efficiency, (b) a power output of 265±15 mW (0.47 W/mm) with 30±3 percent power-added efficiency (both over the 7–11 GHz band), and (c) a power output of 220±45 mW (0.39 W/mm) with 29±4 percent power-added efficiency over the 6–12 GHz band. With a 0.7-μm-gate-length GaInAs MISFET, a small-signal gain of 5±0.5 dB over the 11.4–22.6 GHz band was obtained. These data include all connector, bias network, and circuit losses.**

We also present an equivalent circuit model of 1-μm-gate-length GaInAs MISFET's based on *S*-parameter measurements. The model is essentially that of a MESFET with capacitors representing gate-to-source and gate-to-drain overlap capacitances added at input and output.

I. Introduction

Wide-band amplifiers are important components in many government and commercial systems. These amplifiers require active devices with very high gain–bandwidth products to achieve high performance.

$Ga_{0.47}In_{0.53}As$ lattice matched to SI InP substrates (hereinafter called GaInAs) offers the potential for microwave devices with performance superior to that of GaAs field-effect transistors [1] because of its higher low-field mobility, peak velocity, and intervalley ΓL separation [2]–[5]. Also, GaInAs is an important material for long-wavelength optoelectronics and lasers; thus GaInAs MISFET's should find applications in optoelectronic integrated circuits. The low (~ 0.3 V) barrier height of GaInAs [6] results in poor Schottky diodes, making a technology other than a Schottky barrier gate FET (MESFET) necessary. We have developed metal–insulator–semiconductor FET (MISFET) technology [9]–[12] using low-temperature-deposited SiO_2 as the gate insulator [7], [8] to exploit the potential of GaInAs.

We have developed 1-μm-gate-length, self-aligned-gate (SAG) GaInAs MISFET's operating up to 32.5 GHz [13]. Here, we describe the development and performance of wide-band power and small-signal amplifier stages using these GaInAs MISFET's. An equivalent circuit model of the self-aligned-gate GaInAs MISFET is also presented.

II. Device Fabrication

The GaInAs MISFET's used in this study were fabricated using an SAG process. Such a process is essential to minimize the gate overlap capacitances that impair microwave performance, while maintaining the full-gate structure necessary for good device stability. Details of the SAG process and device characteristics are given in [13].

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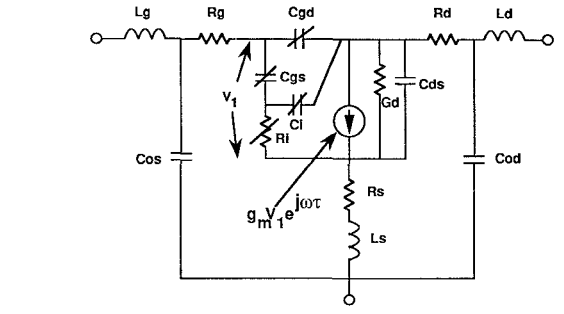
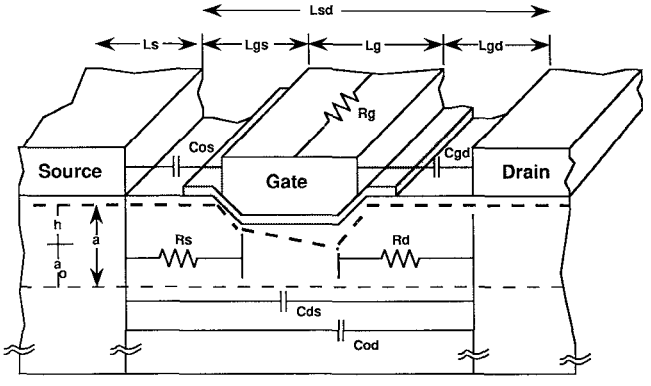


(a)



(b)

Fig. 1. (a) Equivalent circuit and (b) cross section of 1-μm-gate-length, 0.56-mm-gate-width GaInAs MISFET.

III. GaInAs MISFET Equivalent Circuit

The equivalent circuit of our depletion-mode SAG GaInAs MISFET's is based on the GaAs MESFET model and is shown in Fig. 1. This circuit is the MESFET equivalent circuit with two capacitors representing the gate-to-source (C_{os}) and gate-to-drain (C_{od}) overlap capacitances added at input and output, respectively. These capacitances result from the gate overlapping highly doped source and drain regions (full-gate structure) [13]. The equivalent circuit element values are listed in Table I. The parameters C_i and R_i are small and are included for completeness and compatibility with other models.

The circuit element values were derived as follows: The transconductance (g_m) and output conductance (G_d) were obtained from the dc I–V characteristics (note that this provides only an estimate, the ac values being likely to differ from the dc values). The parasitic capacitances C_{ds}, C_{os}, and C_{od} were calculated from the device geometry and materials parameters. The parasitic lead inductances l_g, l_d, and l_s were obtained from studies of package parasitics and from *S*-parameter measurements made on unbiased GaAs MESFET's with similar geome-

tries. Since MISFET's do not have a Schottky gate, Fukui's method [14] cannot be used to determine source (r_s), drain (r_d), and gate (r_g) resistances. Instead, the values of these elements were estimated from values derived from GaAs MESFET's with similar geometries and determinations of ($r_s + r_d$), for the MISFET, by Hsu's method [15].

The remaining element values (C_{gs}, C_{gd}, r_i, and C_i) were determined by computer optimization using the SUPERCOMPACT program. These values were adjusted to minimize the difference between measured and computed S-parameter data over the 8–19 GHz range.

It is interesting to note that the gate and drain lead inductances (l_g and l_d), combined with the gate-to-source and gate-to-drain overlap capacitances (C_{os} and C_{od}), form low-pass filter networks at input and output, respectively. These networks may provide partial matching close to the device.

The overlap capacitances are not the overlap capacitances in the sense referred to for MOS devices. In our MISFET the gate metal does not overlap the source/drain contacts. There is a sidewall capacitance, however, as the n+/n region on the source side overlaps the gate metal (with gate oxide sandwiched in the middle—see Fig. 1). This capacitance has been computed from the device geometry and $C_{os} \sim 0.127$ pF. On the drain side there is a depletion region under the gate with the maximum depletion thickness occurring at the drain edges of the gate. This depletion region will be in series with the oxide. Therefore, the sidewall capacitance is very small and can be neglected. However, there is another capacitance contribution since the oxide layer extends from the source to the drain (with some series resistance). This capacitance was calculated using Pucel's [16] formulas. In order to distinguish it from C_{ds}, normally referred to in the literature, we called it C_{od} (the name overlap capacitance for this may be a misnomer). The calculated value of C_{od} is ~ 0.05 pF and the optimized value from the device model is 0.127 pF. Other parasitic capacitance paths may account for the difference. We did not see any modeled difference when C_{od} was directly connected to ground or when it was connected through the source series resistance.

The equivalent circuit was used to simulate the small-signal gain response of an amplifier with simple LC input and output matching circuits having lossless elements. The simulated gain response showed a small-signal gain of 7 ± 0.5 dB from 7 to 18 GHz, demonstrating the wide-band performance potential of these devices.

IV. GaInAs MISFET Wide-Band Amplifiers

The high-performance potential of GaInAs MISFET's was demonstrated by fabricating and evaluating 7–11 GHz high-efficiency power amplifier and 11.4–22.6 GHz small-signal amplifier stages.

The 7–11 GHz power amplifier stage used a 1-μm-gate-length, 0.56-mm-gate-width SAG GaInAs MISFET flip-chip mounted to a ridge on top of a pallet made from Thermkon (trademark of CMW Inc.). The 7–11 GHz power amplifier configuration and the corresponding equivalent transmission line circuit are shown in Fig. 2(a) and (b), respectively. The test fixture includes biasing networks (not shown) and allows for fine tuning of the input and output circuits.

Figs. 3 and 4 show the output power and the power-added efficiency of an amplifier tuned for (a) highest efficiency and (b) highest power output over the 7–11 GHz band.

The results show (a) a power output of 230 ± 30 mW (0.41 W/mm) with 33 ± 3 percent power-added efficiency and (b) a power output of 265 ± 15 mW (0.47 W/mm) with 30 ± 3 percent power-added efficiency, both over the 7–11 GHz band. Also, a power output of 220 ± 45 mW (0.39 W/mm) with 29 ± 4 percent power-added efficiency was obtained over the 6–12 GHz octave band.

The test fixture contains the necessary dc blocks, biases, and transmission lines. The reported powers and gains are measured at the test fixture's SMA connectors and so reflect actual amplifier performance. Including the ~ 0.5 dB total fixture loss the chip-level power in Fig. 3 is 245 ± 30 mW and the efficiency is 36 ± 3 percent.

Fig. 5 shows the small-signal ($P_{in} \sim 1$ mW) wide-band performance of a more recent, submicrometer gate-length GaInAs MISFET (gate width ~ 0.56 mm, channel oxide thickness ~ 65 nm) mounted in our standard single-frequency power test fixture. Chip tuning on input and output was used to obtain a small-sig-

TABLE I
GaInAs MISFET Equivalent Circuit Element Values

l_g	= 0.240 nH	r_s	= 0.45 Ω	g_m	=	100 mS
l_d	= 0.196 nH	r_d	= 2.0 Ω	τ	=	4.8 ps
l_s	= 0.075 nH	r_g	= 1.15 Ω			
C_{gs}	= 0.650 pF	r_2	= $1/G_d$ = 211Ω			
C_{od}	= 0.127 pF					
C_{os}	= 0.127 pF					
C_i	= 1.19×10^{-4} pF	r_i	= 0.0111 Ω			
C_{gd}	= 0.054 pF					
C_{ds}	= 0.084 pF					

Gate length = 1 μm, gate width = 0.56 mm, t_{ox} = 45 nm.

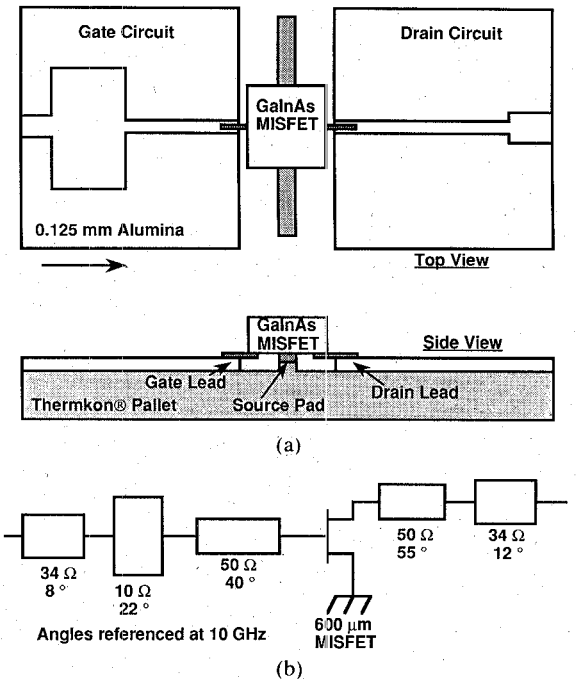


Fig. 2. Typical configuration of 7–11 GHz GaInAs MISFET broad-band power amplifier. (a) Distributed matching elements on 0.125 μm alumina. The tungsten/copper pallet is thermally matched to alumina. The MISFET chip is flip-mounted with gold–tin solder to a ridge on the pallet. The pallet is centered in a test fixture (not shown) which includes bias lines, fine tuning, and SMA connectors. (b) Equivalent transmission lines references to 10 GHz.

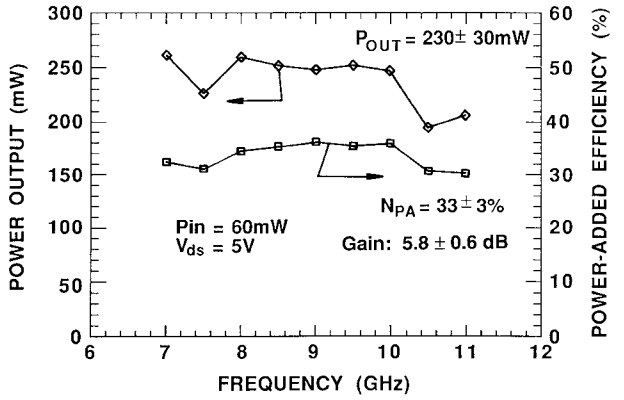


Fig. 3. Power performance of wide-band GaInAs MISFET amplifier stage Tuned for highest efficiency over 7–11 GHz band.

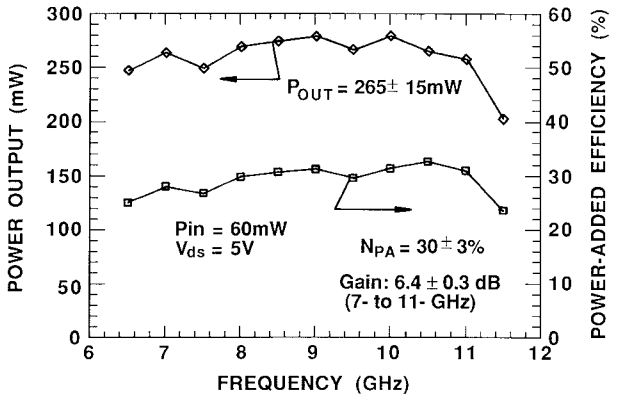


Fig. 4. Power performance of wide-band GaInAs MISFET amplifier stage. Tuned for highest power output over 7–11 GHz band.

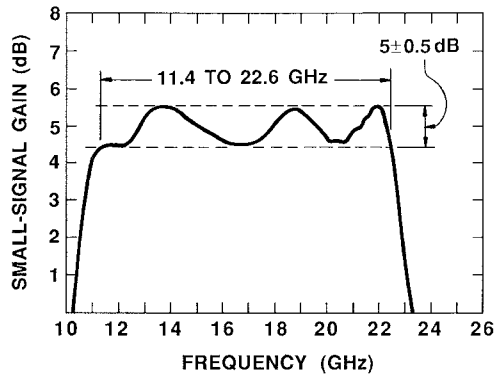


Fig. 5. Wide-band performance of GaInAs MISFET amplifier stage using 0.7-μm-gate-length MISFET.

nal gain of 5 ± 0.5 dB over the bandwidth of 11.4 to 22.6 GHz. Again, no corrections were made for circuit losses.

V. Summary and Conclusions

The combination of high power density, wide bandwidth, and high power-added efficiency obtained demonstrates the potential of GaInAs MISFET's in wide-band amplifier applications. Further development, including submicrometer gate lengths and the use of improved device geometries, will result in significant improvements to the already good performance of GaInAs MISFET wide-band power amplifiers.

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Reactances of Slotline Short and Open Circuits on Alumina Substrate

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***Abstract*—Resonant techniques have been employed in order to determine the equivalent normalized reactance of slotline planar short circuits and open circuits realized on alumina substrates. Data for slotline short circuits are presented in a graph covering a wide range of normalized slot widths. Characteristics of several slotline open circuits are given demonstrating their resonant behavior and the resulting bandwidth limitation. As**

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